METHODS AND APPARATUS FOR TIMING RECOVERY OF VESTIGIAL SIDEBAND (VSB) MODULATED SIGNALS

FIELD OF THE INVENTION

The present invention relates to digital signal processing systems in general, and more particularly to methods and apparatus for timing recovery of vestigial sideband (VSB) modulated signals.

BACKGROUND OF THE INVENTION

The recovery of data from a VSB signal at a receiver requires the implementation of timing recovery for symbol synchronization by which the receiver clock (timebase) is synchronized to the transmitter clock. This permits the received signal to be sampled at the optimum point in time, thus reducing the chance of a slicing error associated with decision-directed processing of received symbol values. Prior-art VSB receivers utilize a known synchronization (sync) pattern to extract timing information from the VSB signal. For example, the Digital Television Standard Document A/55 published by the American Television Standards Committee (ATSC) defines a 4 symbol sync pattern for every 832 symbols transmitted in a VSB signal. Receivers that utilize such sync patterns, such as is described in U.S. Patent No. 5,260,793, typically suffer from a relatively long convergence time as well as convergence to a poor solution where strong and close (less than pattern length) intersymbol interference is present.

The disclosures of all patents, patent applications, and other publications

mentioned in this specification and of the patents, patent applications, and other publications cited therein are hereby incorporated by reference.

SUMMARY OF THE INVENTION

The present invention seeks to provide methods and apparatus for timing recovery of digital vestigial sideband (VSB) signals that overcomes the disadvantages of the prior art described above. A "blind" approach is employed where a baseband VSB signal is filtered by a band-edge filter. The filter output is then transformed using a non-linear transformation and then filtered using a linear filter. The output is then used as a timing correction signal to a digital resampler and/or to an external clock source. In this manner the energy contained in the sampled received signal is maximized. This approach is more responsive to signal reflections in the channel and has a faster acquisition time than do prior art receivers.

There is thus provided in accordance with a preferred embodiment of the present invention apparatus for timing recovery of vestigial sideband (VSB) modulated signals including a narrow band pass filter adapted to receive a baseband VSB signal having a positive-frequency signal edge and provide a portion of the positive-frequency signal edge, and a non-linear transformer adapted to receive the signal portion and provide a timing-retrievable signal adapted for retrieval of timing information therefrom.

Further in accordance with a preferred embodiment of the present invention the apparatus further includes a loop filter adapted to receive the timing-retrievable signal and average the timing-retrievable signal to provide a timing correction signal.

Still further in accordance with a preferred embodiment of the present invention the pass band of the band pass filter generally encompasses the

positive-frequency signal edge, and the center frequency of the positive-frequency signal edge is included in the signal portion.

Additionally in accordance with a preferred embodiment of the present invention the signal portion includes a nonzero band of frequencies of the positive-frequency signal edge frequency.

Moreover in accordance with a preferred embodiment of the present invention the non-linear transformer is adapted to square the signal portion thereby providing a complex signal having a real and an imaginary component and provide the imaginary component as the timing-retrievable signal.

There is also provided in accordance with a preferred embodiment of the present invention a method for timing recovery of vestigial sideband (VSB) modulated signals, the method including filtering a baseband VSB signal having a positive-frequency signal edge to provide a portion of the positive-frequency signal edge, and non-linearly transforming the signal portion to provide a timing-retrievable signal adapted for retrieval of timing information therefrom.

Further in accordance with a preferred embodiment of the present invention the method further includes averaging the timing-retrievable signal to provide a timing correction signal.

Still further in accordance with a preferred embodiment of the present invention the filtering step provides the center frequency of the positive-frequency signal edge included in the signal portion

Additionally in accordance with a preferred embodiment of the present invention the filtering step provides a nonzero band of frequencies of the positive-frequency signal edge frequency included in the signal portion.

Moreover in accordance with a preferred embodiment of the present invention the transforming step includes squaring the signal portion, thereby providing a complex signal having a real and an imaginary component, and providing the imaginary component as the timing-retrievable signal.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be understood and appreciated more fully from the following detailed description taken in conjunction with the appended drawings in which:

Fig. 1 is a simplified graphical illustration of the spectrum of a baseband VSB signal useful in understanding the present invention;

Fig. 2 is a simplified block diagram of a VSB receiver constructed and operative in accordance with a preferred embodiment of the present invention; and

Fig. 3 is a simplified block diagram of the VSB receiver timing block of Fig. 2.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

Reference is now made to Fig. 1 which is a simplified graphical illustration of the spectrum of a baseband VSB signal useful in understanding the present invention as described hereinbelow. A VSB modulated signal is defined herein as a signal of the form $v(t) = \mathrm{Re}\{\sum_n a_n p(t-nT)e^{j2\pi f_c t}\}$, where a_n are the information symbols, $p(t)$ is the modulation pulse shape, f_c is the carrier frequency, T is the symbol period, and $Re\{\}$ represents the real component of a complex number. A baseband VSB signal is defined herein as a complex signal of the form $b(t) = \sum_n a_n p(t-nT)$. A spectrum S of a

baseband VSB signal is shown in Fig. 1, having a positive frequency signal edge 2 and a negative frequency signal edge 4. A negative frequency edge center 6 is defined herein as the signal at a frequency of 0. A positive frequency edge center 8 is defined as the signal at frequency $\frac{1}{2T}$. Note that the negative frequency edge center 6 and the positive frequency edge center 8 are usually the 3DB bandwidth points of the VSB signal.

Reference is now made to Fig. 2 which is a simplified block diagram of a VSB receiver constructed and operative in accordance with a preferred embodiment of the present invention. A VSB modulated signal 10 embodying transmitted data is shown being received by a tuner 12 and down-converted to a signal 12' of an intermediate frequency (IF), preferably a standard IF frequency such as 44 MHz, prior to channel decoding. The down-converted signal 12' is then sampled at an analog-to-digital (A/D) converter 14 to an A/D converted signal 14'. The VSB pilot tone of signal 14' is then detected using a frequency-and-phase-locked loop (FPLL) 16 which locks the carrier frequency and phase and produces an I/Q signal 16' typically comprised of both in-phase (I) and quadrature-phase (Q) signal components. FPLL 16 preferably shifts signal 16' in frequency such that the spectrum of signal 16' appears as spectrum S in Fig. 1.

In one mode of operation FPLL 16 then feeds the I/Q signal 16' to a digital resampler 20 which preferably comprises a digital numerically controlled oscillator (NCO). A timing recovery block 18 then processes a signal 20' output from digital resampler 20 to derive a timing correction signal 18' which may then be fed back to digital resampler 20. Digital resampler 20 may process the I/Q signal 16' received from FPLL 16 using the timing correction signal 18' to derive T-spaced or fractionally sampled signals which are synchronized with the transmitted clock rate embodied in

VSB modulated signal 10. The resampled signal is then fed to a VSB detector 24 which derives the data from the signal.

In an additional or alternative mode of operation FPLL 16 feeds the I/Q signal 16' directly to VSB detector 24, bypassing digital resampler 20. The timing correction signal 18' is then fed to an external clock generator 22 which may be used to drive the A/D converter 14 in synchronicity with the transmitted clock rate.

Additional reference is now made to Fig. 3 which is a simplified block diagram showing timing recovery block 18 of Fig. 2 in greater detail. Signal 20' (Fig. 2), shown in Fig. 3 as input signal $a(k)$ and generally designated 26, is a complex signal having a real component, being the in-phase (I) component described hereinabove with reference to Fig. 2, and an imaginary component, being the quadrature-phase (Q) component. Signal 26 is filtered by a narrow band-pass filter 28 centered at a positive-frequency signal edge 30 of signal 26. Preferably, the pass band of filter 28 generally encompasses positive-frequency signal edge 30, and filter 28 provides a portion of positive-frequency signal edge 30. The signal portion preferably includes the center frequency of edge 30, and most preferably a nonzero band of frequencies of positive-frequency signal edge 30. The output of filter 28, shown in Fig. 3 as signal $x(k)$, is then passed to a non-linear transformer 32 which is preferably a square function that raises to the power of two. The output of transformer 32, when averaged over time, is proportional to the symbol timing offset of the signal 16', and may therefore be used to derive a timing correction signal that may be fed to a digital resampler or an external clock source such as a voltage controlled oscillator (VCXO). To derive the timing correction signal the imaginary component output of transformer 32 expressed by the equation $y(k) = Im\{x(k)^2\}$ is fed to a loop filter 34 which is defined by the following

equations:

$$z(k) = d \cdot y(k) + g(k)$$

$$g(k) = g(k-1) + c \cdot y(k-1)$$

where k is the time index, $x(k)$ is the input to transformer 32, $y(k)$ is the input to the loop filter 34, $z(k)$ is the output of loop filter 34, and c and d are constants. Constants c and d determine the bandwidth and convergence time of the timing loop as is well known in the art for PLLs. Performance may also be affected by the choice of the band pass filter 28, where the narrower the filter, the less noisy the steady state output but with slower convergence.

It is appreciated that the averaging over time of the output of transformer 32 may be accomplished by other known substitutes for loop filter 34 described hereinabove.

As was explained above, digital resampler 20 (Fig. 2) preferably includes a digital numerically controlled oscillator (NCO) that generates the nominal timing instances of the signal and modifies them according to the correction signal $z(k)$. If we denote the timing instances by $t(n)$, then:

$$t(n+1) = t(n) + Tnom + z(k)$$

where $Tnom$ is the nominal time (in samples of the input signal) between output samples. For example, if the input is sampled at 3.4 samples per symbols, and the desired resampler output is 2 samples per symbol, then $Tnom = 3.4/2 = 1.7$. When used in conjunction with an analog VCXO, the VCXO is assumed to be nominally tuned to the nominal sampling frequency of the signal. The VCXO then changes its frequency relative to the nominal frequency by an amount relative to the correction signal input to the VCXO. If we denote the VCXO output frequency by f(t), then:

$$f(t) = Fnom + u \cdot z(k)$$

where *Fnom* is the nominal frequency and u is a constant.

While the present invention has been described with reference to a few specific embodiments, the description is intended to be illustrative of the invention as a whole and is not to be construed as limiting the invention to the embodiments shown. It is appreciated that various modifications may occur to those skilled in the art that, while not specifically shown herein, are nevertheless within the true spirit and scope of the invention.